REMARKS/ARGUMENTS

Claims 1-38 are pending in the application. The Examiner has rejected claims 1-38. Applicant has amended claim 24. Applicant respectfully requests reconsideration of pending claims 1-38.

Applicant has amended claim 24 to correct an error in the preamble. Applicant submits the amendment is merely cosmetic and does not affect the scope of the claims. Applicant submits the amendment does not add new matter.

The Examiner has objected to the abstract as exceeding 150 words. Applicant has amended the abstract. Applicant submits the amended abstract obviates the Examiner's objection to the abstract.

The Examiner has rejected claims 1, 16, 18, 19, 24, 25, 27, 28, 30, 34, 36, 37, and 38 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. As to claim 1, the Examiner states, "claim 1 recites "the key jointly define" (see line 4), which renders the claim indefinite." Applicant respectfully disagrees. Applicant notes claim 1 recites, "...wherein the key-based parity word and the key jointly define a comparand." Thus, Applicant submits the Examiner's rejection of claim 1 has been obviated.

As to claims 16, 18, 19, 24, 25, 27, 28, 30, 34, 36, 37, and 38, the Examiner states such claims "recite the phrase 'adapted for' since languages that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation." Applicant refers the Examiner to MPEP § 2111.04, titled "Adapted to," "Adapted for," "Wherein," and "Whereby" Clauses, which includes the following:

> The determination of whether each of these clauses is a limitation in a claim depends on the specific facts of the case. In *Hoffer v. Microsoft Corp.*, 405 F.3d 1326, 1329, 74 USPQ2d 1481, 1483 (Fed. Cir. 2005), the court held that when a "'whereby' clause states a condition that is material to patentability, it cannot be ignored in order to change the substance of the invention." *Id.* However, the court noted (quoting *Minton v. Nat'l Ass'n of Securities Dealers, Inc.*, 336 F.3d 1373, 1381, 67 USPQ2d 1614, 1620 (Fed. Cir. 2003)) that a "'whereby clause in a method claim is not given weight when it simply expresses the intended result of a process step positively recited.'" *Id.*

Applicant notes the above-cited MPEP section does not describe such clauses as giving rise to a rejection under 35 U.S.C. § 112, second paragraph. Thus, Applicant respectfully requests the Examiner reconsider claims 16, 18, 19, 24, 25, 27, 28, 30, 34, 36, 37, and 38 pursuant to the above-

cited MPEP section. Accordingly, Applicant submits the rejection of claims 16, 18, 19, 24, 25, 27, 28, 30, 34, 36, 37, and 38 has been obviated.

The Examiner has rejected claims 1-38 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Ichiriu (6,597,595). Applicant respectfully disagrees.

As to claims 1 and 12, the Examiner states, "Ichiriu does not explicitly detailed [sic] the aspect of comparing predetermined protection word with the key-based protection word for indicating errors 'as recited in claim 1.'" The Examiner further states, "However, Ichiriu in FIG. 24, teach that a match error detector (705) is a compare circuit that compare [sic] bits of the error address (131) with corresponding bits of the N-bit match index (174) to generate a match error signal 732 (see col. 36, lines 37-67) which the system of Ichiriu is basically employing the same method as the inventor's invention to detect errors." The Examiner continues, "Therefore, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to substitute the method of detecting errors and match error detector of Ichiriu with the claimed method for comparing protection word (CRC word) and error detection." Applicant respectfully disagrees.

Regarding claim 1, while the Examiner acknowledges "Ichiriu does not explicitly detailed [sic] the aspect of comparing predetermined protection word with the key-based protection word for indicating errors 'as recited in claim 1,'" Applicant submits the Examiner does not appear to allege any portion of the cited reference as teaching or suggesting "generating a key-based generating a key-based parity word and a key-based protection word after receiving a key, wherein the key-based parity word and the key jointly define a comparand," as recited in claim 1. Also, Applicant submits the Examiner does not appear to allege any portion of the cited reference as teaching or suggesting "accessing a predetermined protection word corresponding to an address of a CAM module that contains data corresponding to the comparand in response to receiving the address from the CAM module," as recited in claim 1. Thus, Applicant submits the Examiner's proposed modification of Ichiriu still would not anticipate or render obvious the subject matter recited in claim 1.

Furthermore, the Examiner states, "However, Ichiriu in FIG. 24, teach that a match error detector (705) is a compare circuit that compare [sic] bits of the error address (131) with corresponding bits of the N-bit match index (174) to generate a match error signal 732 (see col. 36, lines 37-67) which the system of Ichiriu is basically employing the same method as the inventor's invention to

detect errors." While the Examiner does not appear to allege "bits of the error address (131)" as suggesting "the predetermined protection word" or "corresponding bits of the N-bit match index (174)" as suggesting "the key-based protection word," Applicant is unsure if the Examiner is attempting to allude to such purported analogies. If so, Applicant submits element 174 is described, in column 5, lines 27-29, of the cited reference, as "...a CAM index 174 that points to the address of an empty row of CAM cells within the CAM array (i.e., the 'next free address')." Applicant submits the Examiner has not provided any evidence as to why a "next free address" would purportedly suggest "the key-based protection word." Also, Applicant notes column 5, lines 3-5, of the cited reference state, "Upon detecting an error, the error detector 107 outputs an error address 131 and asserts an error flag signal 132." Applicants submits the Examiner has not presented evidence why, if the error detector 107 of the cited reference has already detected an error, the "bits of error address (131)" would purportedly suggest "the predetermined protection word."

Moreover, the Examiner states as purported motivation to modify the teachings of the cited reference, "...because it would be relatively [sic] and yet high [sic] reliable in operation." Applicant submits the Examiner purported motivation is incomprehensible and, therefore, fails to comply with MPEP §§ 2143 and 2143.01. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness. Accordingly, Applicant submits claim 1 is in condition for allowance.

Regarding claim 12, Applicant notes the Examiner states, "Ichiriu does not explicitly detailed [sic] the aspect of comparing predetermined protection word with the key-based protection word for indicating errors 'as recited in claim 1,'" but does not appear to make any statement with regard to claim 12. Thus, Applicant submits the Examiner has failed to perform the factual inquiry of "2. Ascertaining the differences between the prior art and the claims at issue," described in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), as cited by the Examiner. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness under 35 U.S.C. 103(a). Accordingly, Applicant submits claim 12 is in condition for allowance.

As to claims 2 and 3, the Examiner states, "In addition Ichiriu disclosed that the comparand register (115) is used to store a comparand value received via the comparand bus (143), and outputs the comparand value to the CAM array (101) and in an alternative embodiments [sic] the comparand register may be omitted and the comparand value input directly to the CAM array from the comparand bus (see col. 3 lines 58-64)." However, Applicant notes claim 2 recites "The method of claim 1

wherein the key includes a 28-bit connection identifier." Applicant submits the Examiner appears to fail to allege any portion of the cited reference as purportedly teaching or suggesting the subject matter of claim 2. Therefore, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to claim 2. Thus, Applicant submits claim 2 is in condition for allowance.

As to claim 3, Applicant submits the Examiner appears to fail to cite any portion of the cited reference as allegedly teaching or suggesting, as one example, "...wherein the key-based parity word and the key jointly define a comparand," as recited in claim 1, from which claim 3 depends. Thus, Applicant submits the portion of column 3 of the cited reference noted by the Examiner fails to anticipate or render obvious the subject matter of claim 3 as viewed in the context of claim 1, from which claim 3 depends. Thus, Applicant submits claim 3 is in condition for allowance.

As to claims 4 and 5, the Examiner states, "In addition Ichiriu disclosed in FIG. 6, the compare circuit (208) compares the output of the parity generator (206) with the corresponding stored parity bit. Compare circuit 208 is preferably a combinatorial logic circuit such as an XOR circuit that outputs a logic "1" only if the stored parity bit and the parity bit generated by the parity generator do not match, but may alternatively be any type of circuit for detecting mismatch between the stored and generated parity bits. The outputs of all the compare circuit 208 are logically ORed in gate (221) so that, if any one of the compare circuits 208 signals a mismatch [sic] (see col. 9, lines 33-43)." However, Applicant sees no allegation by the Examiner that any portion of the cited reference teaches or suggests "...wherein generating the key-based protection word includes generating a cyclical redundancy code," as recited in claim 4. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to claim 4. Accordingly, Applicant submits claim 4 is in condition for allowance.

As to claim 5, Applicant sees no allegation by the Examiner that any portion of the cited reference teaches or suggests "...wherein generating the key-based protection word includes generating a bit interleaved parity word," as recited in claim 5. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to claim 5. Accordingly, Applicant submits claim 5 is in condition for allowance.

As to claims 6-11, the Examiner states, "In addition Ichiriu in FIG. 24, teaches that a match error detector (705) is a compare circuit that compare [sic] bits of the error address (131) with

corresponding bits of the N-bit match index (174) to generate a match error signal 732 (see col. 36, lines 37-67)." As to claim 6, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "generating the key-based parity word is performed by a parity word generator of an input protection module," as recited in claim 6. Applicant also submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "generating the key-based protection word is performed by a protection word generator of an output protection module," as recited in claim 6. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 6. Accordingly, Applicant submits claim 6 is in condition for allowance.

As to claim 7, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "storing a plurality of predetermined protection words in memory of the output protection module," as recited in claim 7. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 7. Accordingly, Applicant submits claim 7 is in condition for allowance.

As to claim 8, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting a comparator being "...of the output protection module," as recited in claim 8. Moreover, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "...wherein comparing is performed by a comparator of the output protection module," as recited in claim 8. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 8. Accordingly, Applicant submits claim 8 is in condition for allowance.

As to claim 9, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "searching storage of the CAM module for the address containing data corresponding to the comparand," as recited in claim 9. Also, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "providing the address to the output protection module in response to the address containing data corresponding to the comparand being identified in said storage," as recited in claim 9. Further, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "wherein accessing the predetermined protection word is performed after providing the address to the output protection module," as recited in claim 9. Thus, Applicant

submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 9. Accordingly, Applicant submits claim 9 is in condition for allowance.

As to claim 10, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "receiving an input error notification...," as recited in claim 10. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 10. Accordingly, Applicant submits claim 10 is in condition for allowance.

As to claim 11, as noted above with respect to claim 1, Applicant submits the Examiner has apparently not alleged any portion of the cited reference as teaching or suggesting a "predetermined protection word" or a "key-based protection word." Thus, Applicant submits the Examiner has apparently not alleged any portion of the cited reference as teaching or suggesting "issuing the output error indication in response to said comparing resulting in a determination that the predetermined protection word is different than the key-based protection word," as recited in claim 11. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 11. Accordingly, Applicant submits claim 11 is in condition for allowance.

As to claim 13, as noted above, Applicant submits the Examiner has apparently not alleged any portion of the cited reference as teaching or suggesting a "predetermined protection word" or a "key-based protection word." Thus, Applicant submits the Examiner has apparently not alleged any portion of the cited reference as teaching or suggesting "issuing the output error indication when the predetermined protection word is different than the key-based protection word," as recited in claim 13. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 13. Accordingly, Applicant submits claim 13 is in condition for allowance.

As to claim 14, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "receiving an input error indication...," as recited in claim 14. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 14. Accordingly, Applicant submits claim 14 is in condition for allowance.

As to claim 15, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "...wherein the input error indication is provided by the CAM module to the apparatus comprising at least one of the input error detection module and the output error detection module," as recited in claim 15. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 15. Accordingly, Applicant submits claim 15 is in condition for allowance.

As to claim 16, the Examiner states, "Ichiriu teaches all the subject matter claimed in claim 1 including Ichiriu in figure 1 disclosed a CAM memory (102) coupled to error detector (107) wherein the CAM memory had and input and output." However, Applicant notes claim 16 is an independent claim that does not depend from claim 1. Accordingly, Applicant submits the Examiner's statement that "Ichiriu teaches all the subject matter claimed in claim 1..." does not serve to allege that any portion of the cited reference anticipates or renders obvious the subject matter of claim 16. Applicant submits the Examiner has not set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 16. Accordingly, Applicant submits claim 16 is in condition for allowance.

As to claim 17, the Examiner states, "Ichiriu teaches all the subject matter claimed in claim 16 including Ichiriu in figure 6 disclosed a parity generator for generating parity bits." However, Applicant submits the Examiner fails to cite any portion of the cited reference as allegedly disclosing the "subject matter claimed in claim 16." Rather, even in the Examiner's purported rejection of claim 16, the Examiner states, "Ichiriu teaches all the subject matter claimed in claim 1...," even though claim 16 is an independent claim and does not depend from claim 1. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 17. Accordingly, Applicant submits claim 17 is in condition for allowance.

As to claim 18, the Examiner states, "Ichiriu teaches all the subject matter claimed in claim 16 including Ichiriu in figure 6 disclosed a parity generator for generating parity bits." However, Applicant submits the Examiner fails to cite any portion of the cited reference as allegedly disclosing the "subject matter claimed in claim 16." Rather, even in the Examiner's purported rejection of claim 16, the Examiner states, "Ichiriu teaches all the subject matter claimed in claim 1...," even though claim 16 is an independent claim and does not depend from claim 1. Also, Applicant submit the Examiner appears to fail to allege any portion of the cited reference as supposedly teaching or suggesting, for example, "...the key-based parity word is a cyclical redundancy code." Thus,

Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 18. Accordingly, Applicant submits claim 18 is in condition for allowance.

As to claim 19, the Examiner states, "Ichiriu teaches all the subject matter claimed in claim 16 including Ichiriu in figure 6 disclosed a parity generator for generating parity bits." However, Applicant submits the Examiner fails to cite any portion of the cited reference as allegedly disclosing the "subject matter claimed in claim 16." Rather, even in the Examiner's purported rejection of claim 16, the Examiner states, "Ichiriu teaches all the subject matter claimed in claim 1...," even though claim 16 is an independent claim and does not depend from claim 1. Also, Applicant submit the Examiner appears to fail to allege any portion of the cited reference as supposedly teaching or suggesting, for example, "...the key-based parity word is a bit interleaved parity code." Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 19. Accordingly, Applicant submits claim 19 is in condition for allowance.

As to claim 20, the Examiner states, "Ichiriu teaches all the subject matter claimed in claim 1 including Ichiriu in figure 1 disclosed a comparand register (115) coupled to a CAM memory (101) and further the CAM memory coupled to an error detector (107)." However, Applicant notes claim 20 depends from claim 16, which is an independent claim that does not depend from claim 1. Accordingly, Applicant submits the Examiner's statement that "Ichiriu teaches all the subject matter claimed in claim 1..." does not serve to allege that any portion of the cited reference anticipates or renders obvious the subject matter of claim 16. Also, Applicant submits the Examiner does not appear to allege any cited portion of the cited reference teaches or suggests "...the input error detection module provides the comparand to the CAM module," as recited in claim 20. Thus, Applicant submits the Examiner has not set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 20. Accordingly, Applicant submits claim 20 is in condition for allowance.

As to claim 21, the Examiner states, "Ichiriu teaches all the subject matter claimed in claim 1 including Ichiriu in figure 1 disclosed a comparand register (115) coupled to a CAM memory (101) and further the CAM memory coupled to an error detector (107)." However, Applicant notes claim 21 depends from claim 16, which is an independent claim that does not depend from claim 1. Accordingly, Applicant submits the Examiner's statement that "Ichiriu teaches all the subject matter

claimed in claim 1..." does not serve to allege that any portion of the cited reference anticipates or renders obvious the subject matter of claim 16. Also, Applicant submits the Examiner does not appear to allege any cited portion of the cited reference teaches or suggests "...the output error detection module includes a protection word generator..." or "...the parity word generator performs generating the key-based protection word," as recited in claim 21. Thus, Applicant submits the Examiner has not set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 21. Accordingly, Applicant submits claim 21 is in condition for allowance.

As to claim 22, the Examiner states, "Ichiriu teaches all the subject matter claimed in claim 1 including Ichiriu in figure 1 disclosed a comparand register (115) coupled to a CAM memory (101) and further the CAM memory coupled to an error detector (107)." However, Applicant notes claim 22 ultimately depends from claim 16, which is an independent claim that does not depend from claim 1. Accordingly, Applicant submits the Examiner's statement that "Ichiriu teaches all the subject matter claimed in claim 1..." does not serve to allege that any portion of the cited reference anticipates or renders obvious the subject matter of claim 16. Also, Applicant submits the Examiner does not appear to allege any cited portion of the cited reference teaches or suggests "...the output error detection module includes memory having a plurality of predetermined protection words stored therein..." or "...the predetermined protection word corresponding to the address of the CAM module that contains data corresponding to the comparand is accessed from said memory," as recited in claim 22. Thus, Applicant submits the Examiner has not set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 22. Accordingly, Applicant submits claim 22 is in condition for allowance.

As to claim 23, the Examiner states, "Most of the limitations of these claims have been noted in the rejection of claim 1." However, Applicant notes claim 23 ultimately depends from claim 16, which is an independent claim that does not depend from claim 1. Moreover, Applicant submits claim 1 is a method claim, while claim 23 is an apparatus claim. Applicant submits the Examiner does not appear to have alleged apparatus claim features in the Examiner's rejection of claim 1. As an example, it does not appear to Applicant that the Examiner has alleged any portion of the cited reference as teaching or suggesting "...a comparator connected to the protection word generator and to said memory...," as recited in claim 23. Thus, Applicant submits the Examiner has not set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 23. Accordingly, Applicant submits claim 23 is in condition for allowance.

As to claim 24, the Examiner states, "Most of the limitations of these claims have been noted in the rejection of claim 1." However, Applicant notes claim 24 ultimately depends from claim 16, which is an independent claim that does not depend from claim 1. Moreover, Applicant submits claim 1 is a method claim, while claim 24 is an apparatus claim. Applicant submits the Examiner does not appear to have alleged apparatus claim features in the Examiner's rejection of claim 1. Thus, Applicant submits the Examiner has not set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 24. Accordingly, Applicant submits claim 24 is in condition for allowance.

As to claim 25, the Examiner states, "Most of the limitations of these claims have been noted in the rejection of claim 1." However, Applicant notes claim 25 ultimately depends from claim 16, which is an independent claim that does not depend from claim 1. Moreover, Applicant submits claim 1 is a method claim, while claim 25 is an apparatus claim. Applicant submits the Examiner does not appear to have alleged apparatus claim features in the Examiner's rejection of claim 1. Thus, Applicant submits the Examiner has not set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 25. Accordingly, Applicant submits claim 25 is in condition for allowance.

As to claim 26, the Examiner states, "Most of the limitations of these claims have been noted in the rejection of claim 1." However, Applicant notes claim 23 ultimately depends from claim 16, which is an independent claim that does not depend from claim 1. Moreover, Applicant submits claim 1 is a method claim, while claim 23 is an apparatus claim. Applicant submits the Examiner does not appear to have alleged apparatus claim features in the Examiner's rejection of claim 1. As an example, it does not appear to Applicant that the Examiner has alleged any portion of the cited reference as teaching or suggesting "...means for receiving an input error indication provided by the CAM module in response to failing to find the address corresponding to comparand in storage of the CAM module," as recited in claim 26. Thus, Applicant submits the Examiner has not set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 26. Accordingly, Applicant submits claim 26 is in condition for allowance.

As to claims 27 and 28, the Examiner acknowledges the cited reference "does not explicitly detailed [sic] the aspect of comparing predetermined protection word with the key-based protection word for indicating errors 'as recited in claim 1'." However, Applicant notes claims 27 and 28 are independent claims, and they do not depend from claim 1.

Furthermore, the Examiner states, "However, Ichiriu in FIG. 24, teach that a match error detector (705) is a compare circuit that compares bits of the error address (131) with corresponding bits of the N-bit match index (174) to generate a match error signal 732 (see col. 36, lines 37-67) which the system of Ichiriu is basically employing the same method as the inventor's invention to detect errors." While the Examiner does not appear to allege "bits of the error address (131)" as suggesting "the predetermined protection word" or "corresponding bits of the N-bit match index (174)" as suggesting "the key-based protection word," Applicant is unsure if the Examiner is attempting to allude to such purported analogies. If so, Applicant submits element 174 is described, in column 5, lines 27-29, of the cited reference, as "...a CAM index 174 that points to the address of an empty row of CAM cells within the CAM array (i.e., the 'next free address')." Applicant submits the Examiner has not provided any evidence as to why a "next free address" would purportedly suggest "the key-based protection word." Also, Applicant notes column 5, lines 3-5, of the cited reference state, "Upon detecting an error, the error detector 107 outputs an error address 131 and asserts an error flag signal 132." Applicants submits the Examiner has not presented evidence why, if the error detector 107 of the cited reference has already detected an error, the "bits of error address (131)" would purportedly suggest "the predetermined protection word."

Moreover, the Examiner states as purported motivation to modify the teachings of the cited reference, "...because it would be relatively [sic] and yet high [sic] reliable in operation." Applicant submits the Examiner purported motivation is incomprehensible and, therefore, fails to comply with MPEP §§ 2143 and 2143.01. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness. Accordingly, Applicant submits claims 27 and 28 are in condition for allowance.

As to claims 29 and 30, the Examiner states, "In addition Ichiriu disclosed that the comparand register (115) is used to store a comparand value received via the comparand bus (143), and outputs the comparand value to the CAM array (101) and in an alternative embodiments [sic] the comparand register may be omitted and the comparand value input directly to the CAM array from the comparand bus (see col. 3 lines 58-64)." However, Applicant notes claim 29 recites "The apparatus of claim 28 wherein the key includes a 28-bit connection identifier." Applicant submits the Examiner appears to fail to allege any portion of the cited reference as purportedly teaching or suggesting the subject matter of claim 29. Therefore, Applicant submits the Examiner has failed to set forth a *prima facie* showing

of obviousness with respect to claim 29. Thus, Applicant submits claim 29 is in condition for allowance.

As to claim 30, Applicant submits the Examiner appears to fail to cite any portion of the cited reference as allegedly teaching or suggesting, as one example, "...wherein the key-based parity word and the key jointly define a comparand," as recited in claim 28, from which claim 30 depends. Thus, Applicant submits the portion of column 3 of the cited reference noted by the Examiner fails to anticipate or render obvious the subject matter of claim 30 as viewed in the context of claim 28, from which claim 30 depends. Thus, Applicant submits claim 30 is in condition for allowance.

As to claims 31 and 32, the Examiner states, "In addition Ichiriu disclosed in FIG. 6, the compare circuit (208) compares the output of the parity generator (206) with the corresponding stored parity bit. Compare circuit 208 is preferably a combinatorial logic circuit such as an XOR circuit that outputs a logic "1" only if the stored parity bit and the parity bit generated by the parity generator do not match, but may alternatively be any type of circuit for detecting mismatch between the stored and generated parity bits. The outputs of all the compare circuit 208 are logically ORed in gate (221) so that, if any one of the compare circuits 208 signals a mismatch [sic] (see col. 9, lines 33-43)." However, Applicant sees no allegation by the Examiner that any portion of the cited reference teaches or suggests "...wherein enabling the data processor to facilitate generating the key-based protection word includes enabling the data processor to facilitate generating a cyclical redundancy code," as recited in claim 31. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to claim 31. Accordingly, Applicant submits claim 31 is in condition for allowance.

As to claim 32, Applicant sees no allegation by the Examiner that any portion of the cited reference teaches or suggests "...wherein enabling the data processor to facilitate generating the key-based protection word includes enabling the data processor to facilitate generating a bit interleaved parity word," as recited in claim 32. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to claim 32. Accordingly, Applicant submits claim 32 is in condition for allowance.

As to claims 33-38, the Examiner states, "Most of the limitations of these claims have been noted in the rejection of claim 1." Applicant notes claims 33-38 depend from independent claim 28,

which is an apparatus claim, not from independent claim 1, which is a method claim. Applicant submits claim 28 includes at least one feature which the Examiner did not address with respect to the purported rejection of claim 1. Applicant does not see any assertion by the Examiner that any portion of the cited reference teaches or discloses such at least one feature.

Moreover, the Examiner states, "In addition Ichiriu in FIG. 24, teaches that a match error detector (705) is a compare circuit that compares bits of the error address (131) with corresponding bits of the N-bit match index (174) to generate a match error signal 732 (see col. 36, lines 37-67)." As to claim 33, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "generating the key-based parity word is performed by a parity word generator of an input protection module," as recited in claim 33. Applicant also submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "generating the key-based protection word is performed by a protection word generator of an output protection module," as recited in claim 33. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 33. Accordingly, Applicant submits claim 33 is in condition for allowance.

As to claim 34, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "the data processor program is further adapted for enabling the data processor to facilitate storing a plurality of predetermined protection words in memory of the output error detection module," as recited in claim 34. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 34. Accordingly, Applicant submits claim 34 is in condition for allowance.

As to claim 35, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "...wherein comparing is performed by a comparator of the output error detection module," as recited in claim 35. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 35. Accordingly, Applicant submits claim 35 is in condition for allowance.

As to claim 36, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "searching storage of the CAM module for the address containing data corresponding to the comparand," as recited in claim 36. Also, Applicant submits the

Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "providing the address to the output error detection module in response to the address containing data corresponding to the comparand being identified in said storage," as recited in claim 36. Further, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "wherein accessing the predetermined protection word is performed after providing the address to the output error detection module," as recited in claim 36. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 36. Accordingly, Applicant submits claim 36 is in condition for allowance.

As to claim 37, Applicant submits the Examiner does not appear to cite any portion of the cited reference as purportedly teaching or suggesting "receiving an input error notification...," as recited in claim 37. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 37. Accordingly, Applicant submits claim 37 is in condition for allowance.

As to claim 38, as noted above with respect to claim 28, Applicant submits the Examiner has apparently not alleged any portion of the cited reference as teaching or suggesting a "predetermined protection word" or a "key-based protection word." Thus, Applicant submits the Examiner has apparently not alleged any portion of the cited reference as teaching or suggesting "issuing the output error indication in response to said comparing resulting in a determination that the predetermined protection word is different than the key-based protection word," as recited in claim 38. Thus, Applicant submits the Examiner has failed to set forth a *prima facie* showing of obviousness with respect to the subject matter of claim 38. Accordingly, Applicant submits claim 38 is in condition for allowance.

In conclusion, Applicant has overcome all of the Office's rejections, and early notice of allowance to this effect is earnestly solicited. If, for any reason, the Office is unable to allow the Application on the next Office Action, and believes a telephone interview would be helpful, the Examiner is respectfully requested to contact the undersigned attorney.

Respectfully submitted,

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Date

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